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PROCESSING, FABRICATION, AND DEMONSTRATION OF HTS INTEGRATED MICROWAVE CIRCUITS

Navy Contract No. N00014-91-C-0112

R&D Status Reports – Data Item A001
Report No. 11

Reporting Period: February 1, 1994 through April 24, 1994

Submitted by:

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R&D STATUS REPORT

ARPA Order No.: 7932 Program Code No.: htsc 051-101

Contractor: Westinghouse Electric Corp. (STC)

Contract No.: N00014-91-C-0112 Contract Amount: $6,515,236

Effective Date of Contract: 7/24/91

Expiration Date of Contract: 9/29/95

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Short Title of Work: Processing, Fabrication, and Demonstration of HTS Integrated Microwave Circuits

Reporting Period: 2/1/94 to 4/24/94

DESCRIPTION OF PROGRESS

TASK 1.0: COMPARATIVE TECHNOLOGY ASSESSMENT

This task is essentially complete, but we are continuing to monitor progress in other technologies as they relate to the goals of this program.

TASK 2.1: INTEGRATED SUBSYSTEM SPECIFICATIONS

An EW receiver analysis is currently underway to establish, quantitatively, the benefits of the HTS components being developed in this program. The switched filterbank, the static filterbank and the delay lines, as well as cooled semiconductor components are all being considered as part of this study. The analysis will be completed in the next few weeks and will be reported on next quarter.

TASK 2.2: FUNCTIONAL COMPONENT AND SUBSYSTEM DESIGN, FABRICATION AND TESTING

Filterbanks

In this quarter our efforts have been devoted to optimizing the filterbank channel interconnections using as the vehicle the parallel HTSSE-II program filterbank. The goal was to obtain low-loss, repeatable interconnections which would result in no distortion of the passband of the channels being interconnected. This was accomplished by repositioning the springs that hold the transition chip carrier in place so that they made good ground contact immediately below the microstrip transition line. A test package capable of holding two channels was used for this purpose so as to minimize the number of variables involved. With this arrangement it was possible to measure the effect of only one transition chip on the filter responses for both channels. Also, the superconducting quality of the transition chips was tested directly by measuring their Q in a test fixture that allows capacitive coupling into the transition chips, treating them as microstrip resonators.

Although most of the chips had high Qs, a few were found that were made up of poor quality YBCO. The reasons for this were traced to the first wafers processed and were probably contaminated during fabrication as the process was being optimized. No further instances of contamination has been found in wafers processed subsequently.

The reproducibility of the packaging was then tested by interchanging substrate-carrier assemblies between similar frames. Very good reproducibility was found for several assemblies, as identical features in very good and less-than-desirable filter responses were reproduced in different packages. This qualified our spring contact arrangement and the coaxial interconnection to the package. It revealed, however, that the area of concern was the substrate-carrier interface. This problem will be further analyzed in the next reporting period.

A preliminary investigation was conducted of the possible causes of the suboptimal channel responses obtained to date and a relatively higher loss than expected (1.5 to 2 dB, instead of 0.5 to 0.8 dB). The ground plane connection to the coaxial connector was modelled as a series RLC circuit of arbitrary values. Also an offset between the center frequencies of the two identical filters that form a channel was introduced. The result was inconclusive on the ground plane contact modelling but yielded passbands surprisingly similar to those obtained experimentally when the filter-pair center frequencies were offset by 5 to 15 MHz (from a nominal 4 GHz). In order to try to determine the possible causes for this offset, the effect of the following variables was examined:

Irregular substrate thickness (wedge-shaped substrate)
50-ohm terminations
Dielectric constant (overall and local variations)
Over ion milling (i.e. dielectric pedestal below HTS line)
Variations in line widths and lengths

Realistic parameter variations from their nominal values were used, obtained from independent measurements, whenever possible. The results of this analysis were that a 0.2

to 0.8% local variation (in the most sensitive region of the filter) in the dielectric constant would produce the negative effects observed. This will be further investigated in the next reporting period.

Delay Lines

Measurements between 0 and 20 GHz were made on a 22.5 ns delay line made for the parallel HTSSE-II program. Figure 1 shows the amplitude response obtained on a 1 dB/ division scale. Superimposed to the measured response is a 1 dB-wide band included to enhance the importance of this result. The top curve forming this band is a theoretical calculation using the measured surface resistances of the strip line and the ground planes. It can be shown that when triple-transit is present, as is the case here, the transmission response is degraded by ripple, such that the ripple crests lay on the ideal transmission response. Indeed, as shown in Figure 1, the theoretical calculation envelopes the ripple peaks. It can also be seen that the ripple is less than 1 dB over most of the range from 0 to 18 GHz but that it is higher above. This result shows, nevertheless, that our approach is valid at least to 20 GHz without the introduction of spurious modes seriously degrading the performance.

In the next reporting period, we will work on reducing the ripple amplitude by improving the input/output matching. Figure 2 shows a theoretical calculation of the optimum insertion loss (the surface resistance of all films involved is assumed to be 0.5 mΩ at 10 GHz and 77K) in dB/ns as a function of frequency. It also shows the calculated noise figure. Note that at, say 10 GHz, the calculated loss is 0.05 dB/ns. From Figure 1 the loss measured is 1.5 dB, or 0.07 dB/ns. The film used had surface resistances of 0.42 mΩ (10 GHz, 77K) for the spiral, and 2.2 and 3.8 mΩ for the ground planes, respectively.

HTS Delay Line 22.5 ns Module

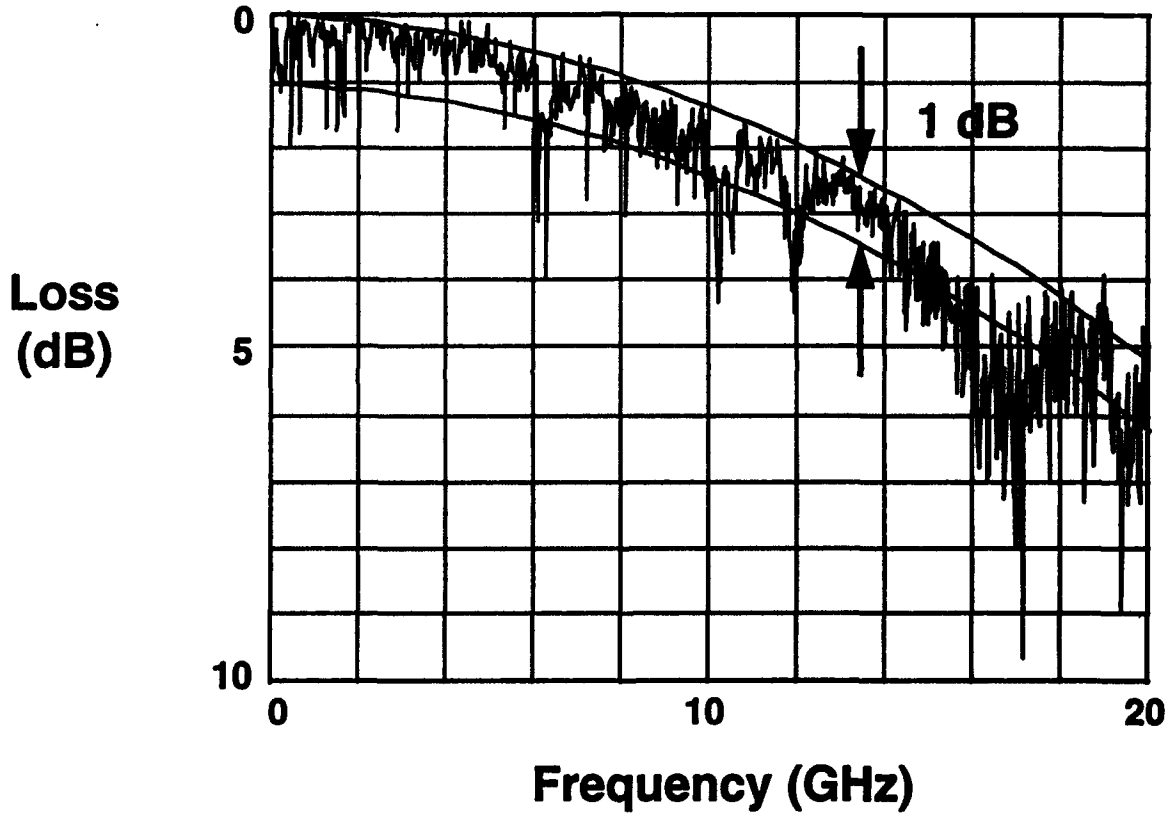

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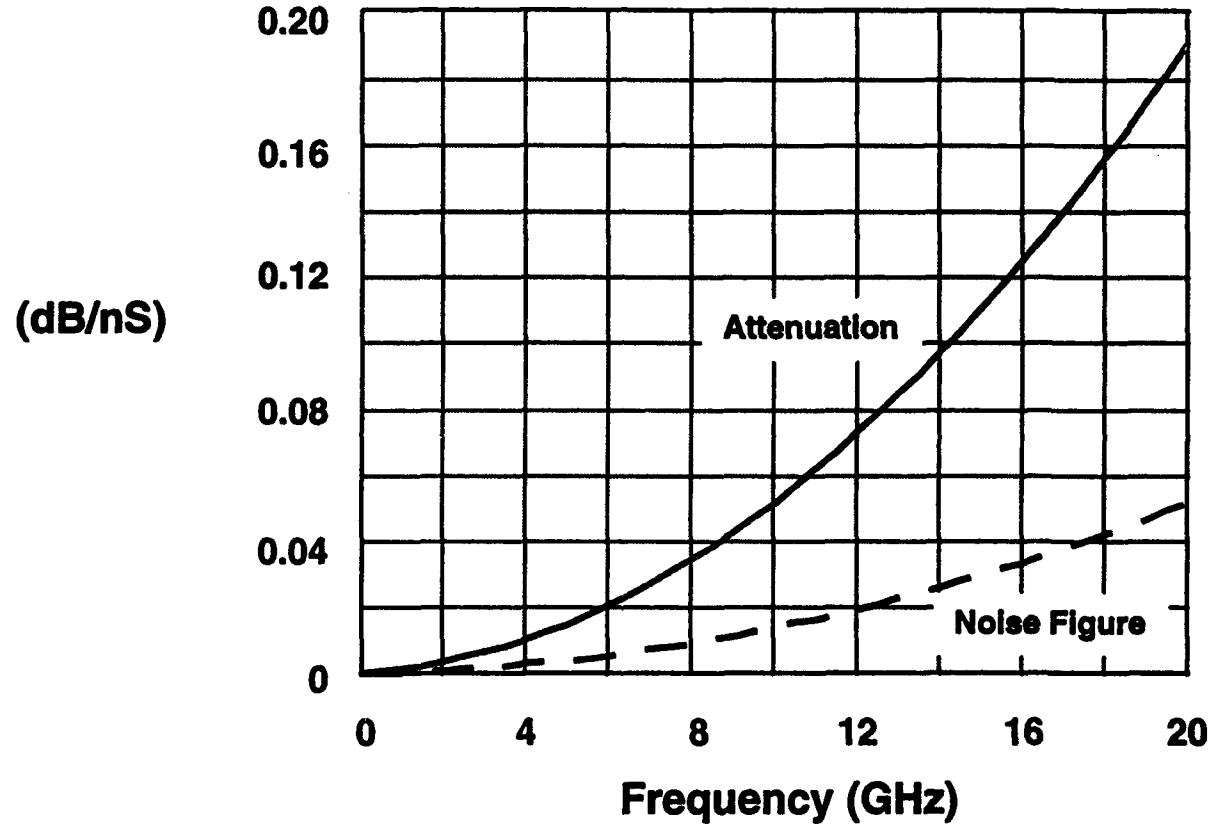
Figure 1 - 22.5 ns YBCO delay line performance between 0 and 20 GHz.

Delay Line Loss and Noise Figure



NOTE: 150 μm-wide stripline and R_s = 0.5 mΩ assumed

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Figure 2 -Calculated insertion loss and noise figure for optimum quality films for both the spiral line and the ground planes.

TASK 3.1: PVD MULTILAYER FILM FABRICATION

The two subtasks scheduled for this reporting period required delivery of YBCO films on both sides of two-inch diameter substrates to Task 2.2, and development of a multilayer deposition capability on four-inch wafers.

Sputter-deposition of YBCO films on 2-inch wafers has stayed ahead of device fabrication requirements. However, the rf surface resistance, R_s, had to be measured for every wafer since the growth process is not sufficiently well-controlled that every wafer will be R_s-qualified. During this quarter, progress was made in controlling the process. The most significant improvement was provided by the vendor of YBCO targets, SSC Inc., which has eliminated the inhomogeneities from targets that can cause the plasma to concentrate at a particular point on the target's surface and burn a hole through the target. When this happened, not only was the target prematurely consumed, the film was degraded since material evaporated from the hole was off stoichiometry. In addition, we reduced the rf power to each sputter source from 85 to 80 W which lowered the growth rate slightly but helped minimize the effect of possible inhomogeneities in the targets. All targets used this quarter eroded uniformly throughout their lifetime and average target lifetime increased to approximately 20 films. During 1993, approximately half of the YBCO targets had a hole burned into them during one of the first few films deposited from the target. Since two sputter sources, and therefore, two targets were used simultaneously to obtain reasonable deposition rates, target changes occurred frequently.

Since sets of 20 films on 2" wafers were obtained without changing targets, it was possible to look for secondary factors that affected run-to-run reproducibility. The most important of these appeared to be differences in either wafer temperature or oxygen pressure that moved the growth conditions away from the decomposition line in the YBCO phase diagram (shown in Figure 8 of Status Report #10). Post-annealing in a diffusion furnace at the decomposition line (800°C and 1 torr of oxygen), where conditions could be reproduced more accurately than in the sputtering chamber, brought high-R_s films down to the same R_s values as the best as-deposited films. An effort is

underway to reduce variations in both wafer temperature and oxygen pressure in the sputtering chamber so that the extra post-annealing step will be unnecessary for all films.

A new sputtering chamber built to a Westinghouse design by Nordiko Ltd., which can accommodate 2, 3, or 4-inch wafers, became fully operational during the quarter. Its operation had been delayed by overheating of vacuum seals during long deposition sequences. Nordiko's latest modifications were successful in giving us a leak-tight system that can withstand the heat load imposed on it. The first three films grown in the new chamber — on 2" wafers — had R_s(77K, 10 GHz) < 1 mΩ (although corrections for film thickness less than a penetration depth had to be made for two of them). In the coming quarter, experiments will be performed to optimize deposition rate followed by growth on larger wafers.

TASK 3.2: MOCVD MULTILAYER FILM FABRICATION

Rapid progress made during the previous quarter on this task continued into this reporting period. YBCO films deposited on both sides of 2" wafers were sent to Westinghouse for R_s measurements. For the first two wafers, the film grown on side A was contaminated by the wafer holder that it faced during growth on Side B so just one side had a low R_s. Subsequent wafers had low R_s films on both sides indicating that the Au-plated wafer holder that was in use cleaned up over time. However, even in these cases, the film on side B was always better than the film on side A. Future work on double sided films will follow the practice at Westinghouse where the first film faces a blank $LaAlO_3$ wafer during growth of the second side instead of facing a Au-plated metal holder.

One of the double-sided wafers coated by MOCVD was used to fabricate a filterbank channel. The transmission response of the completed channel is shown in Figure 3. The R_s(77K, 10 GHz) of the patterned film for this device was 0.65 mΩ. The filter channel results indicate that the films did not degrade during processing or behave differently from sputtered YBCO films in any other way. We have not verified that some

properties, such as linearity and power handling, are comparable to those of sputtered films.

The Ba-thd precursor used at Emcore for all YBCO films grown during the quarter was supplied by Northwestern University. Emcore will not start their evaluation of the new more-volatile precursors, bis(tri-butylcyclo-pentadienyl)barium, (CptBu3)2Ba, and bis(di-butylcyclo-pentadienyl)barium, (CptBu2)2Ba until a backlog of double-sided 2" wafers is produced and a low-R_s 3" film is demonstrated.

Work at Northwestern University has shifted to liquid precursors which offer better long-term vapor-pressure stability simply by maintaining a constant surface area as they sublime. The results of using β-diketonate polyglyme ligands to coordinate the Ba ions have been submitted to the journal, *Chemistry of Materials*, and accepted for publication. The compound has been found to sublime at 150°C and 10^{-6} torr without decomposition. New synthesis routes are being explored to increase the yield of several reaction steps which take a week for completion.

TASK 3.3: RF CHARACTERIZATION OF FILM PROPERTIES

RF surface resistance measurements were made during the quarter on a total of 54 YBCO films on 2-inch wafers for a rate of more than four per week. In contrast to the previous quarter, none of the measurements were used to determine whether specific device processing steps resulted in degradation of film quality. We now have confidence in the processing steps since they were developed with careful monitoring to protect film quality. Instead, the measurements were used either to ensure that sputtered films were qualified for device fabrication or to evaluate films made by MOCVD at Emcore.

The standard measurement of R_s employs a dielectric resonator with a reference YBCO film on a 2" wafer and a film to be measured. Two such resonators are in use with reference films having R_s(77K, 10 GHz) = 0.55 ± 0.04 mΩ and 0.49 ± 0.04 mΩ, respectively. A similar accuracy is expected for low-R_s films (≈0.5 mΩ) and better accuracy for higher-R_s films since losses from the reference film become less significant.

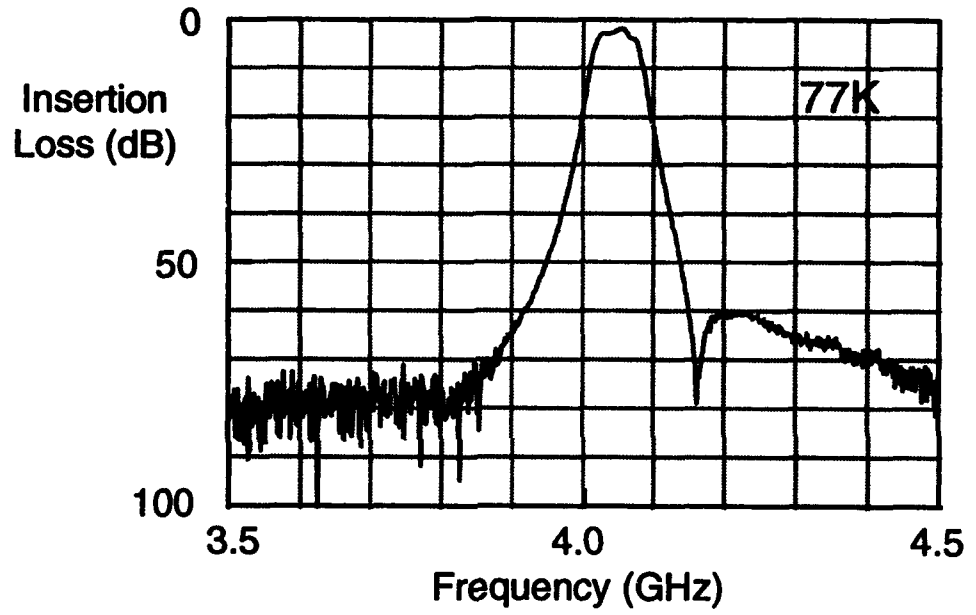

Figure 3. Transmission response for a filter channel fabricated from a 2" wafer coated on both sides with YBCO deposited by MOCVD. The films were qualified by rf surface resistance measurements before processing.

TASK 5.0: SWITCHED FILTERBANK

In this quarter the GaAs Etch-Back FET switches of various designs were integrated into a final mask layout incorporating also several test structures as well as switches with normal FETs. The fabrication of the first masks of the set begun at the end of this reporting period. There was a delay in finalizing the mask design due to a realignment of the test pads, seen as necessary in order to perform cryogenic on-wafer measurements using the probe station at NASA-Lewis. Coaxial on-wafer testing probes have been ordered to match the contact pad location dimensions. Switch fabrication will begin shortly.

PROBLEMS ENCOUNTERED AND/OR ANTICIPATED

Although the start date of this program was July 24, 1991 with the approval of anticipatory spending, the contract was not signed until September 30, 1991 when the first increment of funding was received. The work effort was slowed at DARPA's request to stretch the FY92 funding through 12/31/92. However, FY93 funds were not received until March 30, 1993. These funding limitations have placed the program six months behind schedule.

FISCAL STATUS

Amount currently provided	$5,816,013
Expenditures and commitments through 4/24/94:	4,146,859 *
Funds required to complete:	699,223
FY94 funds required:	None

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* Includes $659,663 committed to subcontractors and purchase orders.